REMARKS

Claims 1-16 are pending in this application. The specification has been amended. Claim 8 has been amended. The drawings have been amended. No new matter has been added by way of this amendment. Reconsideration of the application is respectfully requested.

The specification has been amended on page 4 to clarify that element 305 and Fig. 3a is an exemplary TIS block. The specification has also been amended to illustrate that such a TIS block is also shown in incorporated application Serial No. 09/415,605, which has subsequently issued as U.S. Patent No. 6,297,706. These amendments do not constitute new matter.

Figs. 5b and 5c have been amended to correct an inconsistency disclosed therein. This amendment is similar to the amendment of Fig. 2c that was made in the prior Amendment dated May 2, 2003. Entry of the drawing changes is respectfully requested.

In light of the foregoing amendments and remarks, this application should be in condition for allowance. Early passage of this case to issue is respectfully requested. However, if there are any questions regarding this Response, or the application in general, a telephone call to the undersigned would be appreciated since this would expedite the prosecution of the application for all concerned.

Respectfully Submitted,

Date: May 27, 2003

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COMPLETE SET OF PENDING CLAIMS

1. A latch comprising:

a clocked trans-admittance stage circuit for receiving a voltage and producing a current output; and

an active load connected to receive as input the current output of said trans-admittance circuit and produce a voltage output.

2. The latch in accordance with claim 1, wherein the active load is a trans-impedance stage circuit.

3. The latch in accordance with claim 1, wherein said trans-admittance stage circuit comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors;

a second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and

the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

4. The latch in accordance with claim 3, wherein the base of said first and second transmitters being clocked on opposite phases of a clock signal.

5. The latch in accordance with claim 4, wherein the base of said third transistor receives as input a voltage signal and the base of said fourth transistor receives as input an inverted voltage signal, said third transistor produces a current output signal based on the inverted voltage signal, and said fourth transistor produces an inverted current output signal based on the voltage signal.

6. The latch in accordance with claim 1, further comprising transmission lines coupled between said clocked trans-admittance circuit and said active load.

7. A cascaded latch chain comprising:

a clocked trans-admittance stage latch receiving an input voltage and producing an output current.

8. (Amended) The cascaded latch chain in accordance with claim 7, further comprising at least one latch pair connected to receive the output current of said clocked trans-admittance stage latch and producing an output current, said at least one latch pair including two independent combined trans-admittance and trans-impedance stages.

9. The cascaded latch chain in accordance with claim 8, comprising at least two latch pairs including a first latch pair and a last latch pair, each latch pair having two independent trans-admittance and trans-impedance stages, the two trans-admittance and trans-impedance stages of each latch pair being clocked on opposite phases of a clock signal.

10. The cascaded latch chain in accordance with claim 9, wherein said trans-admittance stage in each latch pair comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors;

a second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

11. The cascaded latch chain in accordance with claim 9, wherein the two trans-admittance and trans-impedance stages in said at least one latch pair are clocked on opposite phases of a clock signal.

12. The cascaded latch chain in accordance with claim 7, further comprising a trans impedance stage latch connected to receive the output current of the last latch pair and produce an output voltage.

13. The cascaded latch chain in accordance with claim 8, further comprising a trans impedance stage latch connected to receive the output current of the last latch pair and produce an output voltage.

14. A latch pair comprising:

two independent combined trans-admittance and trans-impedance stages.

15. The latch pair in accordance with claim 14, wherein each trans-admittance stage comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors;

a second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

16. The latch pair in accordance with claim 14, wherein the two trans-admittance and trans-impedance stages are clocked on opposite phases of a clock signal.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	John Paul MATTIA et al.	Confirmation No.:	7823
Serial No.:	10/033,525	Art Unit:	2816
Filed:	December 28, 2001	Examiner:	LE, Dinh Thanh

For: TRANS-ADMITTANCE TRANS-IMPEDANCE LOGIC FOR INTEGRATED CIRCUITS

MARK-UP FOR SUPPLEMENTAL AMENDMENT OF MAY 27, 2003 PURSUANT TO 37 C.F.R. §1.121

Box Non Fee
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

IN THE SPECIFICATION:

On page 4, delete the third paragraph, and insert the following:

Logic gates configured in accordance with the present invention are less sensitive to transistor collector capacitance and/or wiring capacitance on the collectors of the transistors T3, T4, T5, T6. In addition, the topology shown in Figure 3a provides a convenient node in the

circuit that can be used for input/output connections between logic gates. Specifically, logic gates in accordance with the present invention are arranged to have a TIS input stage and a TAS output stage. Here, element 305 is an exemplary TIS block or latch that is configured in accordance with the present invention. Thus, the current from the switched TAS output is received by the TIS input stage of the next logic block in the cascaded logic chain. A TIS block or latch is also shown in the incorporated U.S. Patent No. 6,297,706, e.g., see element 24 of Figs. 2 and 3. See also, the description at: col. 2, lines 46-54.

IN THE CLAIMS:

8. (Amended) The cascaded latch chain in accordance with claim 7, further comprising at least one latch pair connected to receive the output current of said clocked trans-admittance stage latch and producing an output current, said at least one latch pair including two independent combined trans-admittance and trans-impedance stages.

Respectfully Submitted,

Date: May 27, 2003

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